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(71) Applicant: THE TRUSTEES OF COLUMBIA UNIVERSITY IN THE CITY OF NEW YORK [US/US]; Broadway and 116th Street, New York, NY 10027-6699 (US).

(72) Inventors: TRETZ, Christophe, R.; 533 West 112th Street, New York, NY 10025 (US). WHITE, Robert, C.; 9534 Old Creek Drive, Fairfax, VA 22032 (US).

(74) Agents: TANG, Henry et al.; Brumbaugh, Graves, Donohue & Raymond, 30 Rockefeller Plaza, New York, NY 10112-0228 (US).

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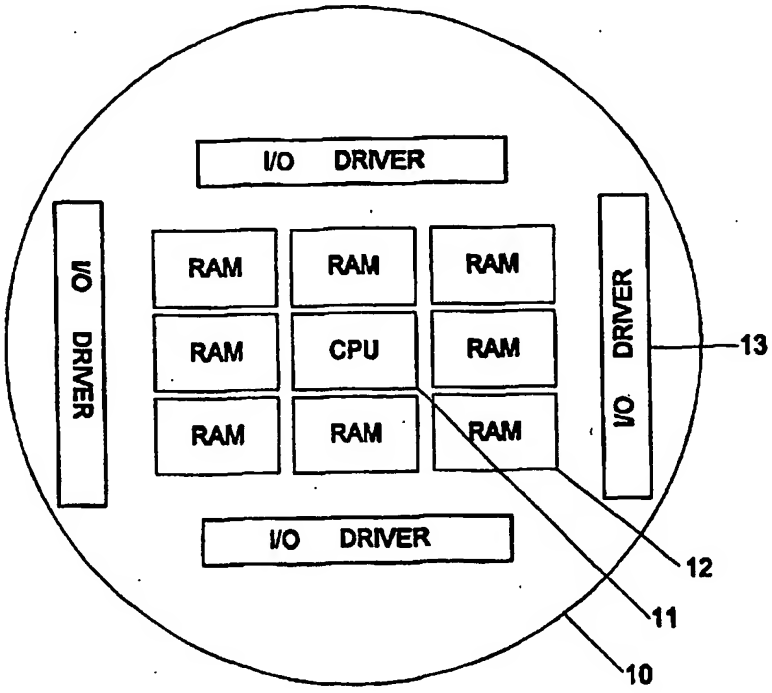
(54) Title: WAFER-SCALE INTEGRATED-CIRCUIT SYSTEMS AND METHOD OF MANUFACTURE

(57) Abstract

With the density of defects which affect device yield being less near the center of a semiconductor wafer (10) than near the periphery, increased yield can be realized in wafer-scale integrated (WSI) circuit manufacture upon placing a more yield-sensitive functional unit at the center of the wafer (10). For example, in a single-chip computer a control processor unit (11) can be integrated with memory arrays (12) surrounding the central processor unit (11).



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Description

Wafer-Scale Integrated-Circuit Systems And Method Of Manufacture

Background of the Invention

The present invention relates generally to semiconductor wafer-scale integrated circuits and, more particularly, to a wafer-scale integrated circuit design and layout technique.

The following published items are representative of proposed wafer-scale integration (WSI) for memory systems:

U.S. Patent No. 5,309,011, issued May 3, 1994 to Tazunoki et al. discloses a packaging technique for wafer-scale integrated memory devices, in which multiple wafers having memory circuits are stacked in a spaced-apart manner and fastened to a pillar passing through the center portion of each wafer. The patent also discloses the use of additional connecting pillars in the peripheral areas of the wafers. In another embodiment, Tazunoki discloses forming a plurality of circuits on a single wafer and describes a technique for interconnecting the circuits. In still another embodiment, the patent discloses a wafer-scale memory arrangement where the central portion of the wafer is filled with memory blocks of substantially the same size and the remaining portion filled with smaller peripheral memory blocks to act as redundant memory to be substituted for any defective central portion memory blocks.

U.S. Patent No. 5,287,472, issued February 15, 1994 to Horst discloses an apparatus for constructing a memory system in a linear array wafer-scale integrated circuit configuration. The memory system contains a plurality of individual, substantially identically

formed memory cells each connected to a neighboring cell by a multiplexer. The multiplexer can be configured to form a linear array of cells that achieves a fixed known delay time from function logic to function logic of the cells.

U.S. Patent No. 5,214,657, issued May 25, 1993 to Farnworth et al. discloses a semiconductor wafer having a plurality of integrated circuit memory sections which are separated from one another by areas called "street areas". Error detection and correction circuitry is provided within the street areas to detect and correct circuit errors generated within the discrete memory sections.

U.S. Patent No. 5,126,828 issued June 30, 1992 to Hatta et al. discloses making cut-outs centrally and/or peripherally to a wafer to allow for an increase in the number of bonding pads for interconnections along the periphery of the wafer. The increase in bonding facilitates communication between circuitry on the wafer and external outside circuitry.

U.S. Patent No. 4,038,648 issued July 26, 1977 to Chesley discloses a self-configurable circuit structure for achieving wafer-scale integration. Additionally, a circuit structure is disclosed which accomplishes wafer-scale integration by using dynamic circuit intercoupling capable of subsequent reconfiguration of the intercoupling structure when malfunctions are detected.

In the manufacture of semiconductor integrated circuits, yield is adversely affected by the presence of microscopic defects at a semiconductor wafer surface, as such defects can result in localized electrical device failure. The following published articles report on related quantitative studies:

F. J. Meyer et al., "Modeling Defect Spatial Distribution," IEEE Transactions on Computers, Vol. 38,

No. 4, April 1989 discloses a center-satellite model for describing the distribution of defects on wafers. The article sets aside the theory that defects are randomly distributed on the wafer and suggests a model of defect clustering or scattering to be used to predict wafer yields.

P. Schvan et al., "Defectivity and Yield Analysis and VLSI and WSI," Proceedings of the IEEE International Conference on Computer Design, pp. 89-92, 1986 discloses a methodology to predict the yield of VLSI (very large scale integration) and WSI circuits. The methodology in the article is based on electrical failure densities measured using standard test circuits and circuit sensitivity obtained by analyzing the circuit layout. A methodology for predicting defects is discussed.

Since concern with defects is particularly acute in WSI, it is understandable that WSI has been proposed for memory devices, designed to have multiple memory arrays with the same structure, and each array having regular internal structure. Such design and internal structure can provide for a large measure of redundancy, as electrical connections can be established or broken for defective arrays to be bypassed in favor of better arrays, and as address remapping can be used to bypass defective portions within an array.

Where there is no regular pattern, as, e.g., in the case of a central processor unit (CPU), such techniques are not applicable, so that yield in manufacture may be expected to be unacceptably low when a CPU is to be included in WSI.

Summary of the Invention

Preferred integrated-circuit design and layout in a WSI-system or -assembly is such that an integrated-circuit portion having greater yield sensitivity, e.g.,

the central processor unit (CPU) of a single-chip microcomputer, is disposed in a central region of the semiconductor wafer substrate. Less yield-sensitive units or blocks, e.g., memory arrays are disposed in a peripheral region complementary to the central region. In this fashion, favorable yield can be achieved in the manufacture of high-performance WSI-systems.

Brief Description of the Drawing

Fig. 1 is a top-view schematic of a single-chip computer in accordance with a preferred embodiment of the invention.

Detailed Description

The single-chip computer of Fig. 1 has a mostly random-logic CPU 11, several RAM arrays 12 coupled to the microprocessor 11, and several I/O drivers 13 connected to the RAM arrays 12 or/and to the CPU 11, all on a common semiconductor wafer substrate 10. Other or further functional components may be included, such as fuses, for example. Advantageously, the substrate wafer has a size or diameter in a range from 2 to 5 inches.

Preferably, for high over-all yield in current practice, integrated-circuit feature size or design rule is in a range from 0.8 to 2 micrometers approximately. Foreseeably, satisfactory yield may be realized with design rules down to approximately 0.35 micrometer. Resulting integrated-circuit assemblies can operate with a power supply in a range from 3 to 5 volts. In operation, such assemblies have desirably low heat dissipation.

The microprocessor 11 is disposed centrally on the wafer substrate, occupying an area of approximately 4 cm^2. The memory arrays 12 are disposed surrounding the microprocessor 11. Each memory array occupies an

area of approximately 4 cm^2 and may have up to 64 Mbits of storage capacity. Thus, with 8 memory arrays, the wafer assembly may have a total capacity of 512 Mbits.

The I/O drivers 13 are also disposed peripherally, surrounding the memory arrays 12 as shown.

Various known fabrication processes for very large scale integrated (VLSI) circuits may be used to fabricate a WSI-circuit in accordance with the present invention. Preferred fabrication processes are those used for complementary metal oxide semiconductor (CMOS) circuits. Such processes are well known, for silicon as well as for compound-semiconductor substrates.

The invention is predicated on the observation that most defects, and especially those affecting pattern processing, tend to be near the periphery of the wafer substrate. In the present case, with a CPU-area free of defects, even if two thirds of the surrounding memory is defective, more than 170 Mbits of on-chip memory remains available. In this exemplary configuration, the amount of on-chip fast memory may be so large so as to reduce the amount of cache or external extended memory that is needed. Also, overall execution speed and throughput are enhanced as most or all system/operating software can be held in local memory.

Yield sensitivity of an integrated-circuit unit in a system may be understood as directly related to the likelihood of operational failure of the unit due to material defects, and indirectly related to the number of similar units which can substitute in performing its function in the system. Thus, a CPU is more yield sensitive than a memory array, and especially so if the CPU is coupled to several memory arrays.

As compared with logic/arithmetic processor units, memory arrays are less critical also in view of their lesser complexity. And a memory array may include

redundant cells which, upon suitable address remapping, can be used as substitutes for defective cells, thereby compensating for defects.

Once a device of the invention has been made, it typically will be subjected to functional testing and, depending on test results, to functional reconfiguring.

Testing of a CPU and of surrounding memory units may involve physical contacting with external probes, of contact pads included for this purpose. Since surface area is not at a premium in a wafer-scale assembly, inclusion of a large number of such pads is practicable. More typically, a number of approximately 20 to 30 pads may be sufficient per assembly.

Testing may also involve the use of software loaded into the assembly via its input pads. Such software may be designed for testing of the CPU, as well as of memory units connected to the CPU. Test results may be read out at the output pads of the assembly, for example.

Reconfiguring may involve physically breaking connections to deficient portions of a memory unit or to a deficient memory unit in its entirety. This typically involves the use of a laser pulse for severing a metallic connection, e.g., in a fuse unit.

Also, reconfiguring typically involves software modifications, e.g., for customary logical memory addresses to be translated into appropriate physical addresses of usable memory units and memory cells. Such translation may then be carried out for each store/fetch memory operation in device use.

Other than as computers for data processing, wafer-scale integrated-circuit systems promise to find use, e.g., in high-speed, low-power multimedia processing and communications systems.

Claims

1. A method for making a wafer-scale integrated-circuit system comprising first and second interconnected integrated-circuit units on a common semiconductor wafer substrate, the first integrated-circuit unit being more yield-sensitive than the second integrated-circuit unit,

the method comprising a step of forming a pattern at a major surface of the semiconductor wafer substrate, wherein

the first integrated-circuit unit is formed in a first, central region of the semiconductor wafer substrate, and

the second integrated-circuit unit is formed in a second, peripheral region of the semiconductor wafer substrate.

2. The method of claim 1, wherein the first integrated-circuit unit comprises a logic/arithmetic unit.

3. The method of claim 1, wherein the second integrated-circuit unit comprises a memory array.

4. The method of claim 3, wherein the second integrated-circuit unit comprises a plurality of memory arrays.

5. The method of claim 1, wherein the second integrated-circuit unit comprises an I/O driver unit.

6. The method of claim 1, wherein the semiconductor wafer substrate has a diameter of at least 2 inches.

7. The method of claim 1, wherein the pattern is formed with feature size in a range from 0.35 to 2 micrometers.

8. A wafer-scale integrated-circuit system comprising interconnected first and second integrated-circuit units on a common semiconductor wafer substrate, the first integrated-circuit unit being more yield-sensitive than the second integrated-circuit unit, wherein

the first integrated-circuit unit is disposed in a first, central region of the semiconductor wafer substrate, and

the second integrated-circuit unit is disposed in a second, peripheral region of the semiconductor wafer substrate.

9. The system of claim 8, wherein the first integrated-circuit unit comprises a logic/arithmetic unit.

10. The system of claim 8, wherein the second integrated-circuit unit comprises a memory array.

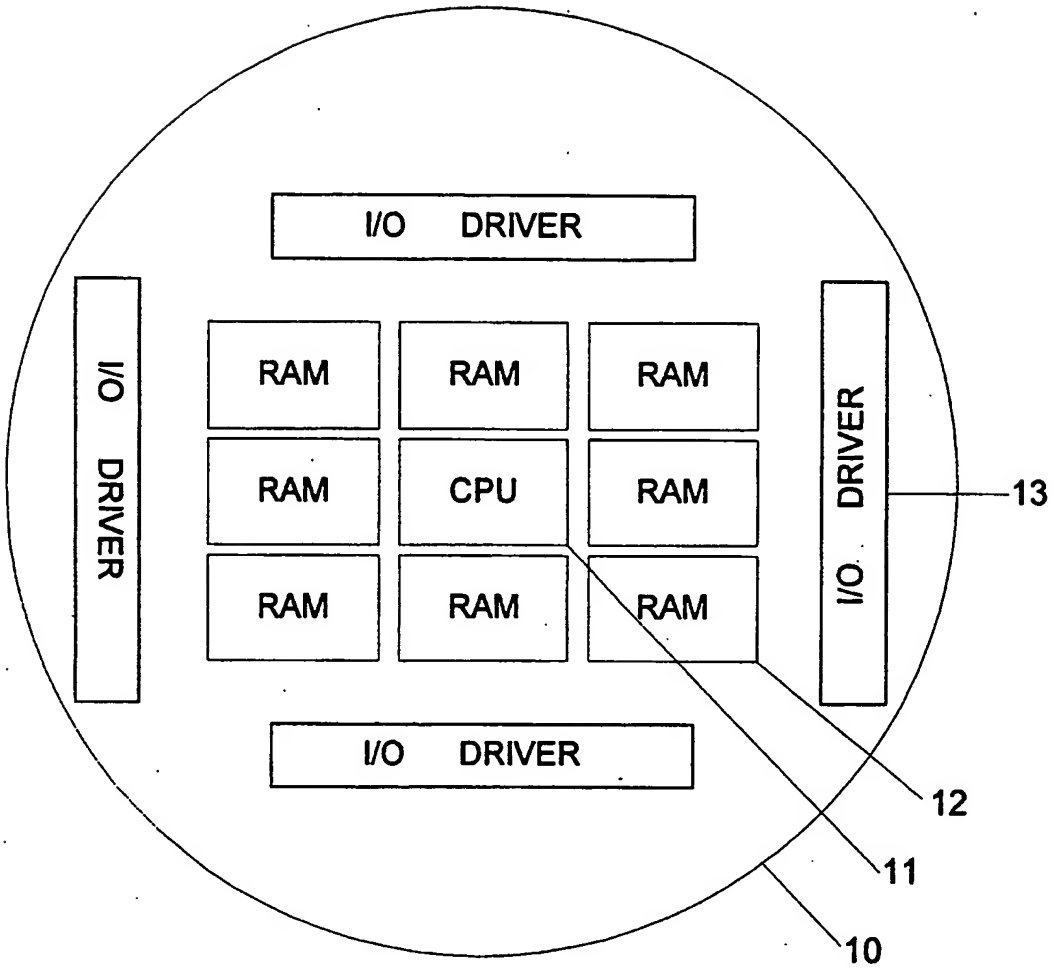
11. The system of claim 10, wherein the second integrated-circuit unit comprises a plurality of memory arrays.

12. The system of claim 8, wherein the second integrated-circuit unit comprises an I/O driver unit.

13. The system of claim 8, wherein the semiconductor wafer substrate has a diameter of at least 2 inches.

14. The system of claim 8, wherein integrated-circuit feature size is in a range from 0.35 to 2 micrometers.

FIG. 1


I/O DRIVER
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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/10005

A. CLASSIFICATION OF SUBJECT MATTER
IPC(6) : H01L 27/10
US CL : 257/202, 203, 208; 437/51
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 257/202-209; 437/51

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
W.R. Runyan and K.E. Bean, Semiconductor Integrated Circuit Processing Technology, Addison-Wesley 1990

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
APS, DIALOG
Search terms: wafer or slice, semiconductor or semiconducting, defect or imperfection or fault, wafer scale or WSI, center or middle or periphery or peripheral

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X/ Y	JP, A, 4-130656 A (Kinoshita) 02 May 1992, English abstract, Fig. 1, and page 353 of Japanese text.	1,3,4,8,10, 11/ 2,5-7,9,12-14
Y	US, A, 5,300,796 (Shintani) 05 April 1994, Fig. 1 and col. 4, lines 15-35.	2, 5, 9, 12
Y/A	W.R. Runyan and K.E. Bean, Semiconductor Integrated Circuit Processing Technology, Addison-Wesley 1990, page 593, 3rd paragraph, and page 637.	6,13/ 1,8
Y	US, A, 5,410,161 (Narita) 04 April 1995, col. 2, lines 49-53.	7, 14

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

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C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US, A, 5,386,129 (Koizumi) 31 January 1995, abstract and Fig. 3.	1, 5, 12